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Built-In self test based on Bit Swapping and Cell Ordering using Low Power Scan Method

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Abstract: A new low power weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme .It supports both pseudorandom testing and deterministic BIST. To implement the low power BIST scheme, a design-for-testability (DFT) architecture is presented. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is used by disabling a part of scan chains.A novel low-power bit-swapping LFSR (BS-LFSR) is used to minimize the transistions, while keeping the randomness almost similar. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycles (or) while scanning out a response to a signature analyzer. These techniques have a substantial effect on average and peak power compared to the existing approach.

Index Terms: Built-In Self-Test, Scan chain, Linear Feedback Shift Register, Bit Swapping, Cell Ordering and Design-for-Testability.

I.INTRODUCTION

Testing becomes a mandatory part of the VLSI industry. Every product must be tested before shipping to the customer. A test is defined as the crucial step to ensure the physical device which is manufactured from synthesized design has no manufacturing defects. The information collected during testing is not only used to remove the defective parts from the product, but it also helps to improve the design and manufacturing process. VLSI testing also improves the manufacturing yield level. Various stages of the VLSI testing are important to designers, product engineers, test engineers, managers, manufacturers, and end-users. A typical test procedure consists of a set of test vectors that are given as input stimuli to the CUT (circuit under test) [2]. The circuits that produce correct response for the set of test vectors is considered as good chips and those circuits that fail to produce correct response are called faulty chips. Testing is performed at various stages of a product/device including the development process, manufacturing process and sometimes even in system level operation. In VLSI industry, various testing techniques are used for testing different types of circuits. Testing of standalone chip is easy with the traditional bed-of-nail methods since all the node points are controllable and observable. This method of testing makes use of a fixture containing a bed-of-nails to access individual devices on the board through test lands laid into the copper interconnect, or other convenient contact points. Testing then proceeds in two phases: the power-off tests followed by power-on tests. Technological development shifts the single ICs to boards and complex designs such as SoCs (system on chip). SoC is heterogeneous in nature. It consists of number of modules collected from different vendors. Conventional bed of-nail method cannot be used for these purposes. Commonly used current testing techniques are as follows ATPG is an electronic design automation (EDA) technique that helps to generate test sequence of a digital circuit, when applied to the manufactured device enables testers to distinguish between the good devices and the faulty devices. These algorithms usually operate with a fault generator program, which creates the minimal collapsed fault list so that the designer need not be concerned with fault generation [3].Controllability and observability measures are used in all major ATPG algorithms. The effectiveness of ATPG is measured by the percentage of modelled defects, or fault models, that are detected by the generated patterns [4]. ATPG algorithms serve different purposes such as generation of test patterns, identification of the redundant circuit logic and checking whether one circuit implementation matches another circuit implementation. ATPG provides high test coverage and fault coverage, but this technique is very expensive.

II.RELATED WORK

DFT techniques are those design techniques that make test generation and test application cost-effective. In other words, they are the design methods that facilitate more thorough and less costly testing. DFT is achieved by adding extra test circuits and this test circuit provides improved access to the internal circuit nodes. It plays an important role in the development of test programs and acts as an interface to test application and diagnosis. DFT is mainly classified into two types: Ad-hoc and Structured DFT methods. Ad-hoc method relies on good design experience to find and fix the problems. It is not used for testing large circuits, since it is an intensive method and does not guarantee good results from ATPG. In Structured DFT techniques, extra logic and signals are added to the circuit so as to allow the test according to some predefined procedure. Commonly used structured methods include scan, partial scan, BIST and

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boundary scan. In the scan design, flip-flops are replaced by the scan flip-flops and connected to form one or more shift registers in the test-mode. A simple scan flip-flop (SFF) using a D flip-flop (DFF) is shown in the Fig 1. A multiplexer is added to the DFF to construct a SFF. Test Enable (TE) signal controls the working of SFF. When TE = 1, DFF works in test mode.SI (scan input) is taken as the input to the DFF. When TE = 0, FF works in normal mode and takes PI (primary input) to the DFF.

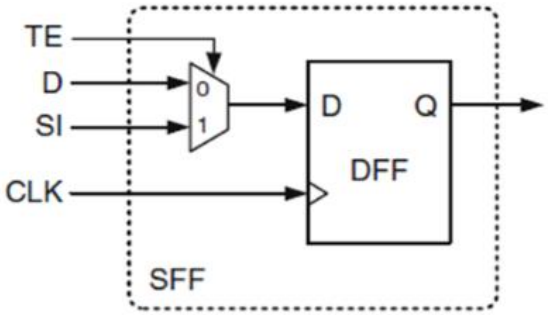

Fig.1 A scan flip-flop (SFF) constructed by D-type flip-flop and multiplexer.

Partial scan is another DFT technique in which only some flip-flops will be converted to SFF during the test mode. The flip-flops for the partial scan are selected on the basis of testability analysis, structural analysis and test generation (Wang, et al., 2007).

Built-in self-test (BIST) is a popular structured DFT technique in which testing is carried out without the requirement of external equipments. In BIST, a portion of the circuit on chip, board or system is used to test the digital logic circuit itself. With technology shrinking into deep submicron or nanometer, traditional ATPG cannot provide high fault coverage to the circuit. BIST remains as a solution for testing circuits that have no direct connections to external pins and have deep hierarchy. It permits an IC to maintain the integrity of its digital logic structures. Logic BIST features are incorporated at the design stage itself. It reduces the dependence on external automatic test equipment (ATE) and thus reducing testing cost. It is classified into two types: Logic BIST (LBIST) and Memory BIST (MBIST). LBIST is used to test logic circuits and MBIST is used to test memory.

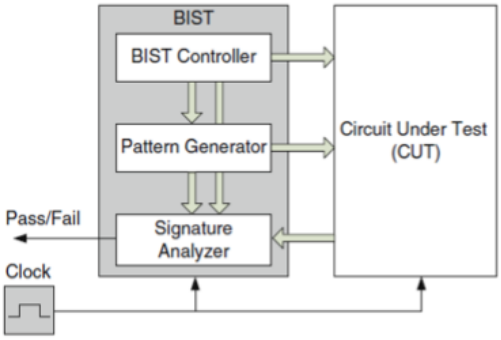

Fig.2 A typical BIST architecture.

A typical architecture of LBIST is shown in the Fig.2. It consists of a test pattern generator (TPG), circuit under test (CUT), BIST controller and ORA (Output Response Analyzer) (Cogswell, 2000). TPG generates pseudorandom test patterns that are given as an input to the CUT. The response from the CUT is collected and is given to ORA. ORA will compact this response into a signature and is compared with the golden signature [1].BIST controller coordinates all the operation among TPG, CUT and ORA. It also has pass/fail indicator.

The main advantage of the BIST method is that it provides at-speed testing, supports concurrent testing and provides improved testability and fault coverage (Agrawal, 2002).

A. Deterministic BIST Method

Deterministic vectors can be encoded into LFSR seeds [5], [6], [7]–[8], [9], [10]], which encoded deterministic vectors into seeds. The requirement on the average size of the LFSR can be reduced by using multiple primitive polynomials [5]. Deterministic vectors were encoded by using a folding counter and compressed by a tree architecture in [6] and [9]. Li and Chakrabarty [9] proposed a reconfigurable scan architecture for effective deterministic BIST. LP design was implemented in the new methodology in [8] to increase the encoding efficiency by combining reseeding and bit fixing.

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The work is about LP delay testing, whose scan architecture and test application scheme are completely different from the new method. Our method is about scan-based BIST for single stuck-at faults based on a new weighted pseudorandom test generator and an LP deterministic BIST approach. The scan architecture in [2] both methods do not require test response shift-out operations, which do not cause zero aliasing. Wen et al. [9], [10] proposed novel X-filling method by assigning 0 and 1 s to unspecified (X) bits in a test cube obtained during ATPG. This method reduces the circuit switching activity in capture mode and can be easily incorporated into any test generation flow to achieve capture power reduction without any area, timing, or fault coverage impact. A new scan shifting method based on the clock gating of multiple groups by reducing the toggle rate of the internal combinational logic. This method prevents cumulative transitions caused by shifting operations of the scan cells, because all scan flip flops are connected to the XOR network for test response compaction.

It is possible to implement LP scan testing in a test compression environment without any increase on test application cost. A new scan architecture to compress test data and compact test responses for delay testing. An important TSV modelling/simulation technique for LP 3-D stacked IC design was presented in [10]. The connectivity of TSVs in many important circuits [5] also needs to be tested in an efficient way.

B. Low Power BIST Methods

A novel low-power BIST technology was proposed in [9] that reduces shift power by eliminating the specified high frequency parts of vectors and also reduces capture power. Multi cycle tests support test compaction by allowing each test to detect more target faults. The ability of multi cycle broadside tests to provide test compaction depends on the ability of primary input sequences to take the circuit between pairs of states that are useful for detecting target faults. This ability can be enhanced by adding DFT logic that allows states to be complemented in [8]. A new DFT scheme for launch-on-shift testing was proposed in [9], which ensures that the combinational logic remains undisturbed between the interleaved capture phases, providing computer-aided-design tools with extra search space for minimizing launch-to-capture switching activity through test pattern ordering. Complete fault coverage can be obtained [9] when the pseudorandom test generator is modified. A combination of a pseudorandom test generator and a combinational mapping logic was constructed by Chatterjee and Pradhan [9] to produce a given target pattern set of the hard-to-detect faults.

III.PROPOSED BS-LFSR AND CELL ORDERING

The proposed BS-LFSR for test-per-scan BIST is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

1) The bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions.
2) The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG.
3) In the BS-LFSR, consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4$, . . . , $cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced.
4) The proposed BS-LFSR has been combined with a cell-ordering algorithm that reduces the number of transitions in the scan chain while scanning out the captured response.
5) The problem of the capture power (peak power in the test cycle) will be solved by using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture power).
6) Triggering architecture has three modes of operation: Shift, Trigger, and Normal. The Shift and Trigger modes are used for testing, while the Normal mode is used for normal operation of the Circuit.
7) In the Shift mode, the Enable signal is low (inactive) and the DR flip-flops remain unchanged. Therefore, the required data can be shifted in the TR chain with no effect on the contents of the DR flip-flops.
8) In the Trigger mode, the Enable signal is high (active) and the multiplexer selects the input connected to the Q output of DR flip-flops. If the XOR output is 0, the DR flip-flop value will not change. If the XOR output is 1, the value of the DR flip-flop is inverted. Therefore, in the Trigger mode, a 1 at the XOR output of a cell causes an inversion of the value stored in its DR flip-flop. This is accomplished by storing different values in the TR flip-flops of this cell and its neighbouring cell (to the left).
9) 9) In the normal mode, the TR chain is loaded with a sequence of alternating 1s and 0s (1010 . . .). This activates the outputs of all XORs; by selecting the normal input of the multiplexer and setting the Enable signal to the desired value, each cell performs its normal operation. The loading process of the TR chain with 1010. . .is performed only

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once, that is, when the test process is completed and the circuit starts its normal operation. During the test, each new vector is obtained through a vector update cycle.

III. CHARACTERISTICS OF BS-LFSR

There are some important features of the proposed BS-LFSR that make it equivalent to a conventional LFSR. The most important properties of the BS-LFSR are the following.

1) The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0or1at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG. Furthermore, the output of the multiplexer depends on three different cells of the LFSR, each of which contains a pseudorandom value. Hence, the expected value at the output can also be considered to be a pseudorandom value.

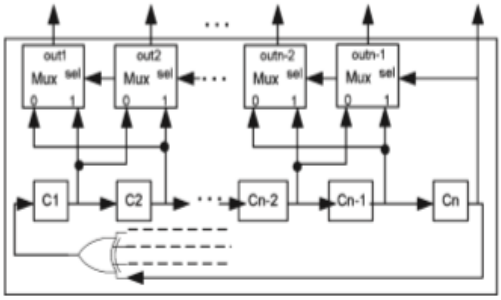


Fig.3 BS-LFSR for test-per-clock BIST.

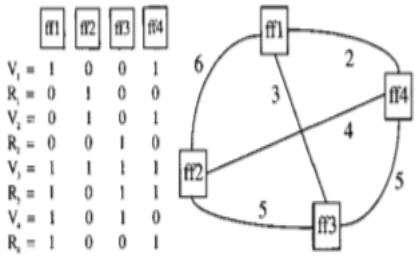
2) If the BS-LFSR is used to generate test patterns for either test per-clock BIST or for the primary inputs of a scan-based sequential circuit (assuming that they are directly accessible) as shown in Fig. 3, then consider the case that c1 will be swapped with c2 and c3 with c4,...,cn−2 with cn−1 according to the value of cn which is connected to the selection line of the multiplexers . In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced by 25% [32].

IV. SCAN CHAIN CELL-ORDERING ALGORITHM

Test power can be minimized by appropriately ordering the scan cells of a given scan chain. The inputs to the proposed procedure are i) a given set of scan flip-flops and ii) a sequence of deterministic test vectors with the corresponding output responses. The output is an ordered scan chain with minimum test power. To tackle this NP-hard problem efficiently, the heuristic procedure operates in two steps: the first one consists in determining the chaining of scan cells, the second one consists in identifying the input and output scan cells of the scan chain. These two steps are described in details.

A. Determining Cell Ordering

The first step of the scan cell ordering procedure consists in determining the order in which the scan cells have to be connected to minimize the occurrence of transitions in the scan chain during scan-in and scan-out operations. To this end, we first consider the set of scan vectors (test vectors and output responses) used during scan testing, and we assume an initial order for the scan flip-flops. More formally, we assume that flip-flop 1 corresponds to bit 1 of each scan vector, flip-flop 2 corresponds to hit 2 of each scan vector , .,,, flip-flop n corresponds to hit n of each scan vector. For example, consider the test sequence shown in Fig. 4, which is composed of four test vectors (VI to V4) and four output responses (R1 to R4). The scan chain has four flip-flops, hence scan vectors are four-bit long. The initial order of the scan cells in the scan chain is depicted on the figure. According to the above description, flip-flop 1, denoted as ffl, corresponds to bit 1 in each scan vector, flip-flop 2, denoted as ff2, corresponds to bit 2, and so on (Figure 2.a).



4 a) 4 b)

Fig.4 Test sequence of scan cell-ordering example.

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The total number of hit differences between each pair of scan flip-flops, which represents the number of transitions that may be generated in the corresponding portion of the scan chain by connecting these two flip-flops together. For the example in Fig.4, calculating the total number of bit differences between each pair of flip-flops (on the complete sequence of test vectors and output responses) provides the following results: d(ffl,ff2) = 6, d(ffl,ff3) = 3, d(ffl,ff4) = 2, d(ff2,fB) = 5, d(ff2,ff4) = 4, d(ff3,ff4) = 5. From these values of the bit differences between flip-flops, it is then possible to construct a complete undirected graph in which each vertex represents a flip-flop and each edge represents a possible connection between two flip-flops (Fig.4.b). The weight on each edge of the graph represents the total number of bit differences between two flip-flops for the complete test sequence, and reflects the number of transitions that may be generated in the corresponding portion of the scan chain by connecting these two flip-flops together. From this weighted graph, the problem then amounts to finding an Hamiltonian cycle of minimum cost in the graph.

The cost of a cycle is obtained by summing the weights on edges belonging to this cycle. This problem is equivalent to the well-known Traveling Salesman Problem, which is well known to be NP-hard (the number of possible solutions is (n-l)!/2 - n being the scan chain length) and for which different polynomial-time approximation algorithms can be used [2]. Among these solutions, greedy algorithms represent a good trade-off between computation time and efficiency of the computed solution. We therefore implemented an heuristic solution based on a greedy algorithm (with a complexity equal to O(n*)) to find the scan cell chaining that minimizes the occurrence of transitions in the scan chain during scan-in and scan-out operations. The greedy algorithm starts from an initial state which is always scan cell ffl in our case (it is reported in that the choice of the initial state is not so crucial in a greedy algorithm considering the number of vertices in the graph to be sufficiently high). Next, the algorithm operates in such a way that, at each stage of decision, a subset of the scan cells is dealt with and considered as definitively assigned.

A. Input and Output Scan Cells Identification

The scan flip-flops, the second step of the ordering shown in (fig.5) procedure consists in defining both the input scan cell and the output scan cell of the scan chain. Appropriately defining the input and output scan cells allows to minimize the propagation of transitions in the scan chain during shifting operations.

Fig.5 Cyclic Graph Orientation.

The weighted transitions and evaluate the n possible sets of scan vectors that each corresponds to a given cutting solution. For example, considering the test sequence given in Figure 4.a, the four possible sets of scan vectors which are evaluated to determine the less power consuming scan chain are shown in Fig.5. Note that in each set, the first, third, fifth and seventh vectors are the test vectors. The remaining scan vectors are the output responses. For each set of scan vectors in Fig.4, i.e. for each possible scan chain. This number represents the number of weighted transitions in test vectors and output responses plus the number of weighted transitions due to opposite values between the first hit of a test vector and the last bit of the previous output response. In this example, the lowest value of WTCotd is 23 and is obtained from the first possible scan chain. Hence, this scan chain (ffl-ff4- ff2-ff3) is the less power consuming scan chain, and ffl is identified as the input scan cell and ff3 as the output scan cell.

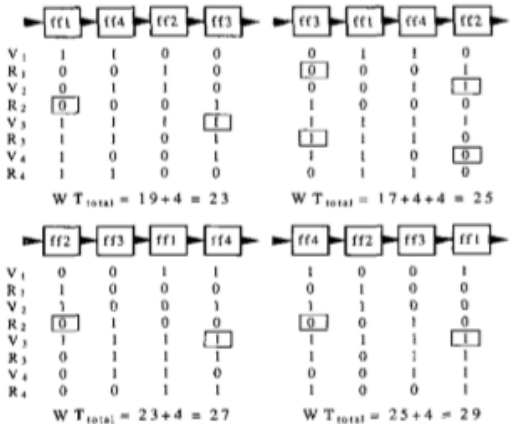

Fig.6 Input and Output scan cells identification.

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IV.ARCHITECTURE OF TESTING

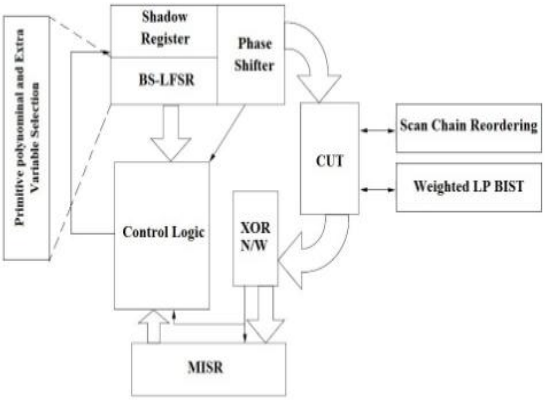

Fig.7 DFT Architecture of BIST

A new scheme to select the size of the BS-LFSR and the number of extra variables simultaneously in order to minimize the amount of deterministic test data. Usually, a small BS-LFSR constructed by a primitive polynomial is sufficient when a well-designed PS is adopted in the pseudorandom testing phase. In our method, (Fig.7) shows a combination of a small BS-LFSR and the PS is used to generate test patterns in the pseudorandom testing phase. The weighted test-enable signal-based pseudorandom test generator generates weighted pseudorandom test patterns. The size of the BS-LFSR is not determined by the maximum number of care bits for any deterministic test vector. That is, the same BS-LFSR is used for both phases. For any degree less than 128, it is computationally feasible to generate enough primitive polynomials in reasonable time, out of which one (whose degree is equal to the maximum number of care bits in the deterministic vectors) can be selected to encode all deterministic test vectors. The tool that we used to generate primitive polynomials can only handle polynomials up to degree 128 of the word-length limit of the computer. However, only very small BS-LFSRs are used for all circuits according to all experimental results (no more than 30).

V. CONCLUSION

The proposed TPG is used to generate test vectors for test-pattern BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. A group of experiments was performed on full-scan ISCAS'89 benchmark circuits. In the first set of experiments, the BS-LFSR shown in [1] is evaluated regarding the length of the test sequence needed to achieve a certain fault coverage with and without the scan-chain-ordering algorithm. For each benchmark circuit, the same numbers of conventional LFSR and BS-LFSR patterns are applied to the full scan configuration.

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